Amendments To the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (original): A switch coupled between a plurality of host units and a device for routing frame information therebetween and comprising:

a. a first serial advanced technology attachment (ATA) port, [including a route aware] capable of receiving a frame information structure (FIS) coupled to a first host unit;

b. a second serial ATA port, [including a route aware] capable of receiving a FIS, coupled to a second host unit;

c. a third serial ATA port, [including a route aware] capable of receiving a FIS, coupled to a device; and

d. an arbitration and control circuit for selecting one of the first host or second host units to [be coupled to] concurrently access the device, through the switch, by accepting commands, from either of the first or second host units, at any given time, including when the device is not in an idle state and whenever either one of the first or second host units sends FIS to the device and further wherein the FIS of the first and second host units and the device identify which one of the first or second host units is an origin and/or destination host so that routing of FIS is transparent to the switch thereby reducing the complexity of the design of the switch rendering its manufacturing less expensive.

Claim 2 (original): A switch as recited in claim 1 wherein said device is a storage unit.

Claim 3 (original): A switch as recited in claim 1 wherein said switch is employed in an enterprise system.

Claim 4 (original): A switch as recited in claim 1 wherein said arbitration and control circuit causes concurrent access of the device by the first and second host units.

Claim 5 (original): A switch as recited in claim 1 wherein a bit is used to indicate which host is the origin or destination of the FIS.

Claim 6 (original): A switch as recited in claim 1 wherein said first, second and third ports are layer 2 ports.

Claim 7 (original): A switch as recited in claim 1 wherein the switch provides for 'route aware' routing.

Claim 8 (currently amended): A switch as recited in claim 1 wherein the switch [switches between layer 2 and] further includes a dual ported first-in-first-out (FIFO).

Claim 9 (currently amended): A switch comprising:

a. a first serial advanced technology attachment (ATA) port, [including a route aware] capable of receiving a frame information structure (FIS), for connection to a first host unit;

b. a second serial ATA port, [including a route aware] capable of receiving a FIS, for connection to a second host unit;

c. a third serial ATA port, [including a route aware] capable of receiving a FIS, for connection to a device, the switch for routing frame information between the first and second host units and the device; and

d. an arbitration and control circuit for selecting either the first host unit or the second host unit to [be coupled to] concurrently access the device, through the switch, by accepting commands, from either of the first or second host units, at any given time, including when the device is not in an idle state, when either one of the first or second host units sends FIS to the device,

wherein while one of the first or second host units is coupled to the device, through the switch, the other one of the first or second host units sends FIS to the switch for routing to the device and further wherein the FIS of the first and second host units and the device identify which one of the first or second host units is an origin and/or destination host so that routing of FIS is transparent to the switch thereby reducing the complexity of the design of the switch rendering its manufacturing less expensive.

Claim 10 (currently amended): A switch as recited in claim 9 wherein [the switch is a serial ATA switch] the switch provides for 'route aware' routing.

Claim 11 (original): A switch as recited in claim 9 wherein said device is a storage unit .

Claim 12 (original): A switch as recited in claim 9 wherein said switch is employed in an enterprise system.

Claim 13 (original): A switch as recited in claim [1] 9 wherein said arbitration and control causes concurrent access of the device by the first and second host units.

Claim 14 (currently amended): A switch that is connectable to a first host unit, a second host unit and a device via serial advanced technology attachment (ATA) links, for routing frame information between the first and second host units and the device, said switch comprising:

a. a first serial ATA port, [including a route aware] capable of receiving a frame information structure (FIS), for connection to a first host unit;

b. a second serial ATA port, [including a route aware] capable of receiving a FIS, for connection to a second host unit;

c. a third serial ATA port, [including a route aware] capable of receiving a FIS, for connection to a device;

d. an arbitration and control circuit for selecting one of the first or second host units to [be coupled to] concurrently access the device through the switch, by accepting commands, from either of the first or second host units, at any given time, including when the device is not in an idle state, when either the first or second host units sends FIS to the device,

wherein while one of the first or second host units is coupled to the device, the other one of to the first or second host units sends FIS to the switch for routing to the device and further wherein the FIS of the first and second host units and the device identify which one of the first or second host units is an origin and/or destination host so that routing of FIS is transparent to the switch thereby reducing the complexity of the design of the switch rendering its manufacturing less expensive.

Claim 15 (original): A switch as recited in claim 14 wherein the switch is a serial ATA switch.

Claim 16 (original): A switch as recited in claim 14 wherein said device is a storage unit.

Claim 17 (original): A switch as recited in claim 14 wherein said switch is employed in an enterprise system.

Claim 18 (original): A switch as recited in claim 14 wherein said arbitration and control circuit causes concurrent access of the device by the first and second host units.

Claim 19 (currently amended): A method for communication between multiple host units and a device, through a serial advanced technology attachment (ATA) switch coupled to the multiple host units and the device using serial ATA links routing frame information therebetween, comprising:

a. [coupling a first serial ATA port,] receiving [including a route aware] a frame information structure (FIS) through a first serial ATA port, [to] from a first host unit [for connection to the switch];
b. [coupling a second serial ATA port, including a route aware] receiving a FIS, [to] through a second serial ATA port, from a second host unit [for connection to the switch];
c. [coupling a third serial ATA port, including a route aware] receiving a FIS through a third serial ATA port [, for connection to a device];
d. arbitrating between the first and second host units and the device;
e. selecting one of the first or second host units for coupling to the device through the switch when either of the first or second host units sends commands for execution by the device;
f. coupling the device to the selected one of the first or second host units; and
g. while the selected one of the first or second host units is coupled to the device, the other one of the first or second host units sending FIS to the switch for routing to the device

during the sending step g., the FIS of the first and second host units and the device identifying which one of the first or second host units is an origin and/or destination host so that routing of FIS is transparent to the switch thereby reducing the complexity of the design of the switch rendering its manufacturing less expensive.

Claim 20 (new): A method for communication, as recited in claim 19, further including the steps of transmitting a frame information structure (FIS) through the first serial ATA port, transmitting a frame information structure (FIS) through the second serial ATA port, and transmitting a frame information structure (FIS) through the third serial ATA port.